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Design of low-power CMOS transceiver front end for 2.4-GHz WPAN applications

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Abstract. This paper describes the design of low-power direct conversion transceiver front end for WPAN (Wireless Personal Area Network) applications using TSMC 0.13 μm CMOS technology. Subharmonic mixers are proposed to mitigate the drawbacks of DC offset problem in direct conversion receiver and injection locking problem in direct conversion transmitter. The receiver front end comprises a low-noise amplifier (LNA), balun and subharmonic mixer. The direct conversion transmitter front end adopts a subharmonic passive mixer, differential to single-ended converter, driver and power amplifier. The post-layout simulation results produce voltage gain of 29 dB, noise figure of 5.84 dB, IIP3 of − 12 dBm and 1.79 mW consumption power for receiver front end at a supply voltage of 0.8 V. The transmitter front end achieves conversion gain of 15 dB, 0 dBm output 1-dB compression point (OP1dB) and 4.27 mW power consumption.

Keywords. Low-noise amplifier; subharmonic mixer; power amplifier; CMOS.

1. Introduction

The Low-Rate Wireless Personal Area Network (LR-WPAN) applications are increasing in our daily life such as automation and control, monitoring, asset tracking, security, etc. [1]. In LR-WPAN, the 2.4-GHz physical layer of the IEEE 802.15.4 standard attracts a lot of focus from the wireless industry. The emergence of LR-WPAN applications is continuously increasing the demand of System-on-Chip (SOC) products using CMOS technology. The advantages of CMOS technology have increased the need for recent research on low-power RF transceivers. To provide a longer battery life, low-power circuit techniques are essential to reduce power consumption in LR-WPAN transceiver front end while obtaining optimal performance.

Among the receiver architectures, low-intermediate frequency (IF) and direct conversion receiver architectures are widely preferred for low-cost, low-power WPAN applications [2, 3]. Low-IF architecture is very attractive for low-power WPAN receivers since it combines the advantages of heterodyne and direct conversion architectures [4, 5]. Choi *et al* [6] designed the merged low-noise amplifier (LNA) and folded mixer with multiple-gated transistor for high-linearity low-IF receiver. The poly-phase filter (PPF) after mixer was designed for achieving − 30 dBc of image rejection and − 4 dBm IIP3 at 5.4 mW power. A low-IF structure still requires a high-resolution analogue-to-digital conversion (ADC) with high sampling rate, which leads to increased design complexity and high power consumption. For these reasons, direct conversion architecture is used in WPAN receivers due to its simple structure, low power and high integration [7]. However, a direct conversion receiver has many drawbacks such as flicker noise, DC offset, I/Q mismatch, even-order distortion and local oscillator (LO) leakage. Syu *et al* [7] designed the direct conversion receiver and concentrated only on the flicker noise problem. For achieving low-flicker-noise performance, vertical NPN bipolar transistors were used in the LO stage of the Gilbert mixer to eliminate the device flicker noise. The noise figure of front end achieved 3.2 dB and 8.1 mW power consumption. Some receiver works are focused only on the front end circuits for achieving low power consumption [8–10]. Srinivasan *et al* [8] produced 8 dB of voltage gain, noise figure of 8.9 dB and 2.88 mW power consumption. It attained low power but the voltage gain was decreased. Cornetta *et al* [9] achieved the gain of 16.7 dB, low noise figure of 2.27 dB and 14.6 mW power consumption. The gain and noise figure performances were improved at high power dissipation. Fiorelli *et al* [10] provided 30 dB conversion gain (CG), 7.5 dB DSB noise figure, − 12.8 dBm IIP3 and 4.7 mW power consumption at 1.2 V supply. The limitation of receiver is that good trade-off between performances is not achieved, particularly in terms of power consumption.

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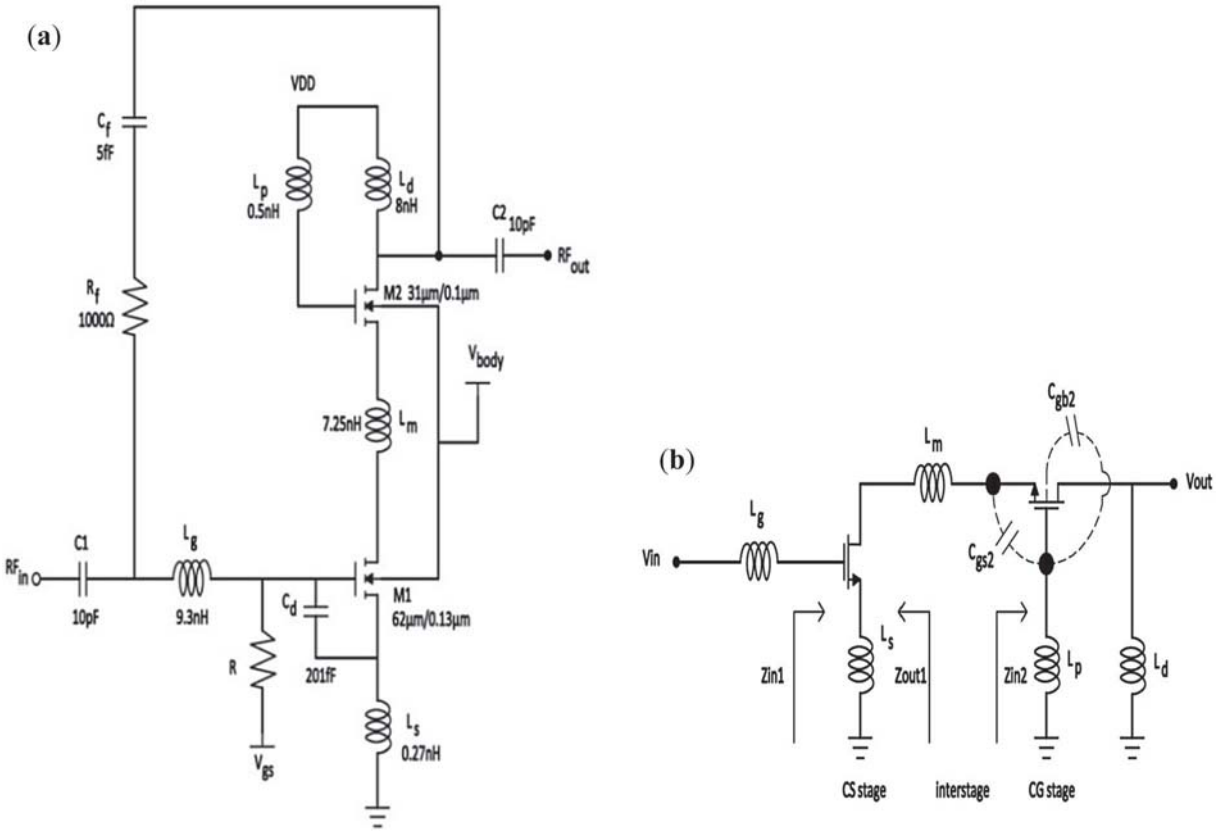

Figure 1. **(a)** Proposed low-noise amplifier. **(b)** Small-signal equivalent circuit.

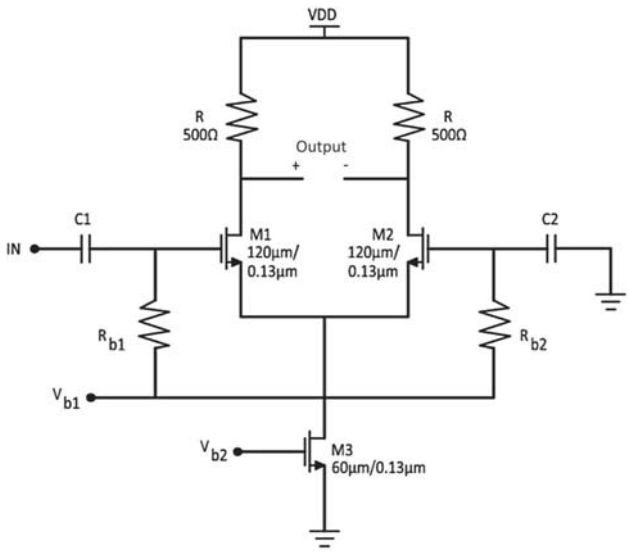

Figure 2. Schematic of active balun circuit.

For WPAN transmitters, direct modulation and direct conversion transmitters are widely used. The limitation of direct modulation technique is external filtering required for noise suppression [11]. For achieving high integration and eliminating external components, a direct conversion transmitter was chosen for the WPAN transmitter. The major drawbacks of the direct conversion transmitter are LO pulling and carrier leakage problems. In [12], circuit techniques were employed for achieving low-power transmitter front end, which utilized current mode circuits instead of voltage mode circuits to improve the linearity of transmitter front end at low supply voltage and low power of 5 mW. It achieved low power, but did not concentrate on the drawback of transmitter. The receiver and transmitter front ends presented in the literature still dissipate high power while obtaining good performance and concentrating on the architecture's drawbacks.

Direct conversion transceiver architecture offers advantages such as simple, on-chip integration and low power consumption due to the absence of IF stage over other architectures. In this paper, based on low power, a direct-conversion architecture is selected for WPAN receiver and transmitter. The important drawbacks of DC offset problem in direct conversion receiver and LO pulling problem in direct conversion transmitter are focused. In circuit level, low-power circuit techniques such as current reuse, folded technique and push pull circuit are utilized in front ends to achieve low-power transceiver front end. Section 2 describes the proposed receiver front end. Section 3

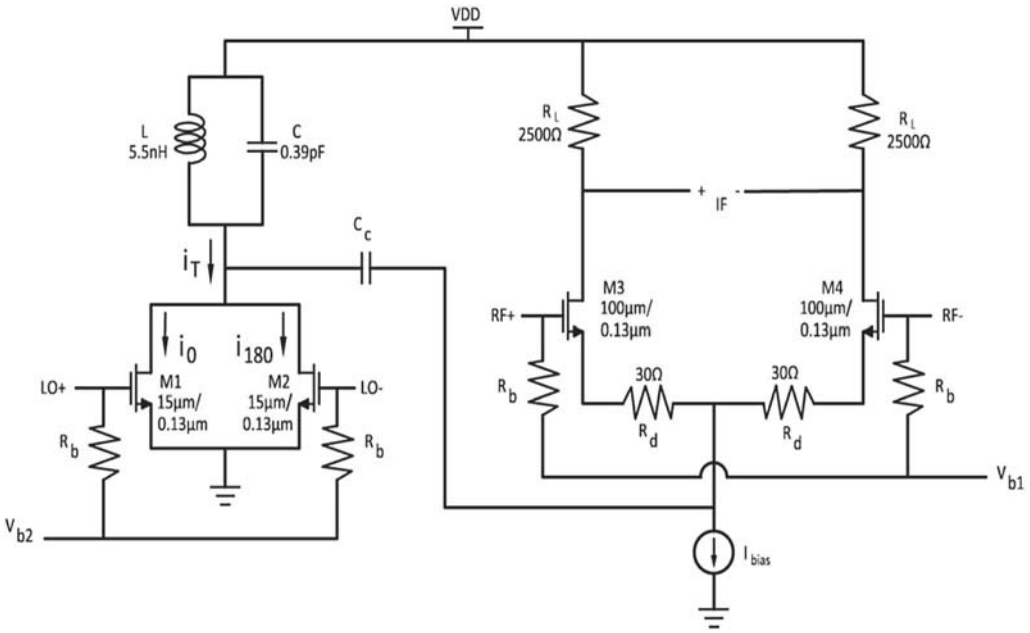

Figure 3. Differential LO subharmonic mixer.

discusses the proposed transmitter front end. Results and discussion are presented in section 4. Conclusion is presented in section 5.

2. Proposed receiver front end

Direct conversion architecture is more suitable for low-cost and low-power WPAN transceiver. In order to avoid the main drawbacks of DC offset problem due to LO leakage and LO pulling problem in direct conversion transceiver, subharmonic mixers are used instead of conventional mixers. Receiver front end circuits such as LNA, balun and subharmonic downconversion mixer are designed and their performances are analysed. Low-power techniques such as current reuse and folded techniques are used.

2.1 *LNA*

An inductively degenerated common source low-noise amplifier (IDCLNA) is more suitable for narrow-band applications. IDCLNA is also used to achieve good gain and low-noise figure at any given amount of power dissipation. When designing this IDCLNA at low power, the performances are degraded. To improve good performance of IDCLNA or cascode LNA such as gain, noise figure, input matching and stability at low power, a modified IDCLNA is proposed. A schematic of proposed LNA is shown in figure 1a. For supporting low supply voltage and low power consumption, FBB (Forward Body Bias) technique is adopted for reducing the threshold voltage from 0.43 to 0.347 V, thereby reducing the supply voltage from 1.2 to 0.8 V. This LNA is operated at 0.8 V. Figure 1b shows the small-signal equivalent circuit of LNA. In this design, cascode LNA acts as a Common Source–Common Gate (CS–CG) two-stage LNA. The CS stage is properly designed for input impedance matching and good noise figure. The cascode transistor (M2) of CG is used for reducing the miller effect, improving the input–output isolation and increasing the output impedance. The bias voltage (V_{gs}) is particularly chosen in the moderate inversion region. The additional capacitance C_d is used to reduce the gate-induced noise. Input and output matching networks are used for providing good return losses and isolations.

An intermediate inductor L_m is added between the CS–CG for improving the matching between two stages.

From figure 1b, the parasitic capacitance is given by

$$C_p = C_{gs2} + C_{gb2} \quad (1)$$

where C_{gs2} is gate to source capacitance and C_{gb2} is gate to bulk capacitance. The parasitic capacitance C_p decreases the gain of CS stage and increases the noise figure of CG stage. An inductor L_P is added at the gate of the CG stage so that it forms the parallel network with C_p to improve the noise figure of CG stage. The inductor L_P cancels out the capacitive effect C_p at a resonant frequency. The modified resistive capacitive feedback network (C_f and R_f) is connected to increase the stability factor. The LNA draws 1.196 mA current from 0.8 V supply.

2.2 *Active balun*

Active balun circuit is needed for producing differential LNA signals. Among the various active balun topologies, differential amplifier topology is designed as shown in figure 2.

The differential amplifier topology increases the gain of LNA. This balun circuit is biased in moderate inversion region. It consumes 0.342 mW power at 0.8 V supply voltage.

2.3 *Subharmonic downconversion mixer*

A schematic of differential LO subharmonic mixer is shown in figure 3. It uses differential LO signals (LO+ and LO−). In this design, RF and LO ports are exchanged in conventional mixer. At the bottom of the mixer, LO signals are applied, and RF signals are applied at the top. The IF output is taken from the RF stage. Initially the differential LO signals are applied at the gates of two NMOS transistors, and these signals are used to generate the $2f_{LO}$ signal. This $2f_{LO}$ current signal is injected into the sources of RF NMOS transistors, which generate the IF signal. The RF transconductance and LO switching stages are coupled via AC coupling capacitor C_c.

The coupling capacitor is used to block the DC signal between these stages. The tail current bias (I_{bias}) is provided by the 500 Ω resistance. The differential LO signals are applied to the gates of M1 and M2 transistors with relative phase difference of 180°. To describe the operation of frequency doubling, consider a small-signal nonlinear drain current, which can be modelled by

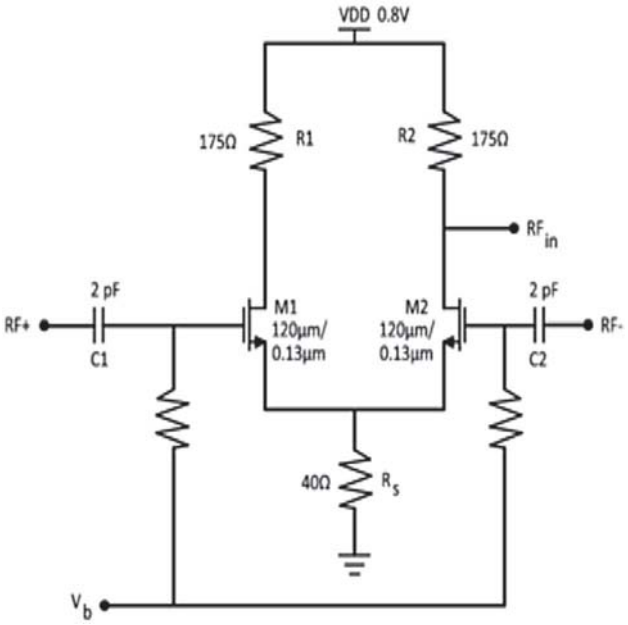

Figure 5. Schematic of differential to single-ended converter.

$$i_d = g_1 v + g_2 v^2 + g_3 v^3 + \cdots \tag{2}$$

where g_1, g_2 and g_3 are, respectively, the main transconductance, second and third-order nonlinear coefficients. The differential LO signals are expressed as follows:

$$v_{LO,0}(t) = A\cos\omega_{LO} t \tag{3}$$

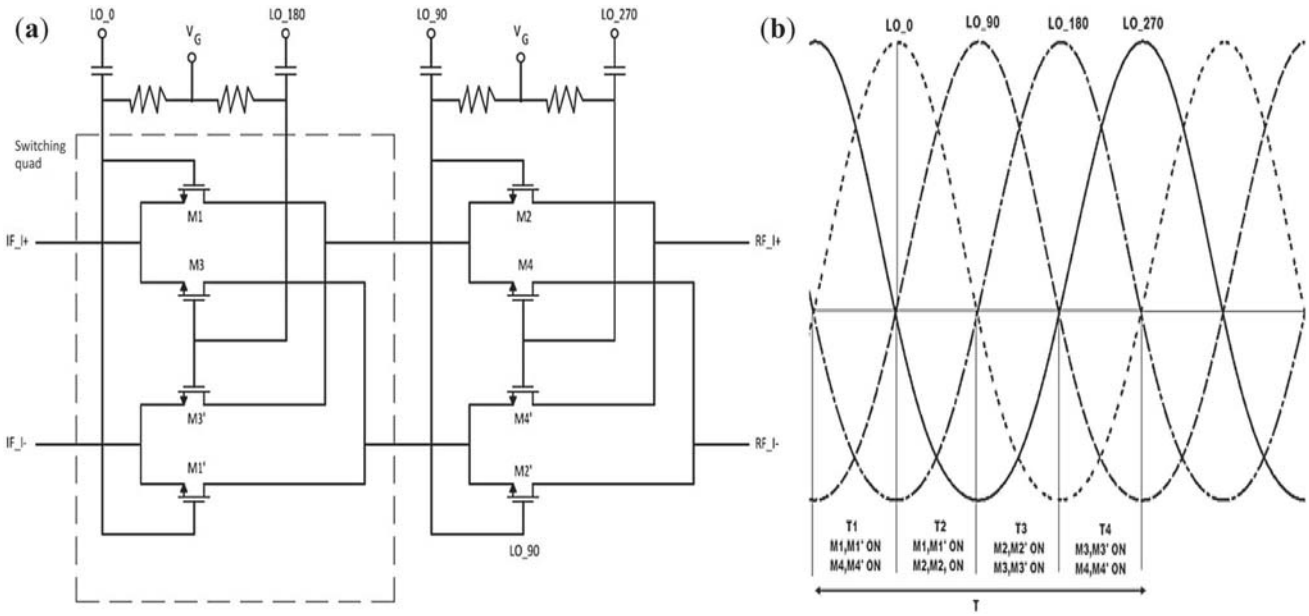

Figure 4. (**a**) Subharmonic upconversion mixer. (**b**) Quadrature LO phases.

$$v_{\mathrm{LO},180}(t) = A\cos(\omega_{\mathrm{LO}} + 180)t = -A\cos\omega_{\mathrm{LO}}t \quad (4)$$

where A is the amplitude of the LO signal. Using the short-channel model, the currents generated by the LO voltages are given by

$$\begin{aligned} i_0 &= g_1 A\cos\omega_{\mathrm{LO}}t + g_2A^2\cos^2\omega_{\mathrm{LO}}t + g_3A^3\cos^3\omega_{\mathrm{LO}}t + \cdots \\ &= g_1 A\cos\omega_{\mathrm{LO}}t + g_2A^2\left[\frac{\cos 2\omega_{\mathrm{LO}}t + 1}{2}\right] \\ &\quad + g_3A^3\left[\frac{\cos 3\omega_{\mathrm{LO}}t + 3\cos\omega_{\mathrm{LO}}t}{4}\right] + \cdots \\ &= \frac{g_2A^2}{2} + \left(g_1A + \frac{3g_3A^3}{4}\right)\cos\omega_{\mathrm{LO}}t \\ &\quad + \left(\frac{g_2A^2}{2}\right)\cos 2\omega_{\mathrm{LO}}t + \left(\frac{g_3A^3}{4}\right)\cos 3\omega_{\mathrm{LO}}t + \cdots \end{aligned} \quad (5)$$

$$\begin{aligned} i_{180} &= -g_1A\cos\omega_{\mathrm{LO}}t + g_2A^2\cos^2\omega_{\mathrm{LO}}t - g_3A^3\cos^3\omega_{\mathrm{LO}}t + \cdots \\ &= g_1A\cos\omega_{\mathrm{LO}}t + g_2A^2\left[\frac{\cos 2\omega_{\mathrm{LO}}t + 1}{2}\right] \\ &\quad + g_3A^3\left[\frac{\cos 3\omega_{\mathrm{LO}}t + 3\cos\omega_{\mathrm{LO}}t}{4}\right] + \cdots \\ &= -g_1A\cos\omega_{\mathrm{LO}}t + g_2A^2\left[\frac{\cos 2\omega_{\mathrm{LO}}t + 1}{2}\right] \\ &\quad - g_3A^3\left[\frac{\cos 3\omega_{\mathrm{LO}}t + 3\cos\omega_{\mathrm{LO}}t}{4}\right] + \cdots \\ &= \frac{g_2A^2}{2} - \left(g_1A + \frac{3g_3A^3}{4}\right)\cos\omega_{\mathrm{LO}}t \\ &\quad + \left(\frac{g_2A^2}{2}\right)\cos 2\omega_{\mathrm{LO}}t - \left(\frac{g_3A^3}{4}\right)\cos 3\omega_{\mathrm{LO}}t + \end{aligned} \quad (6)$$

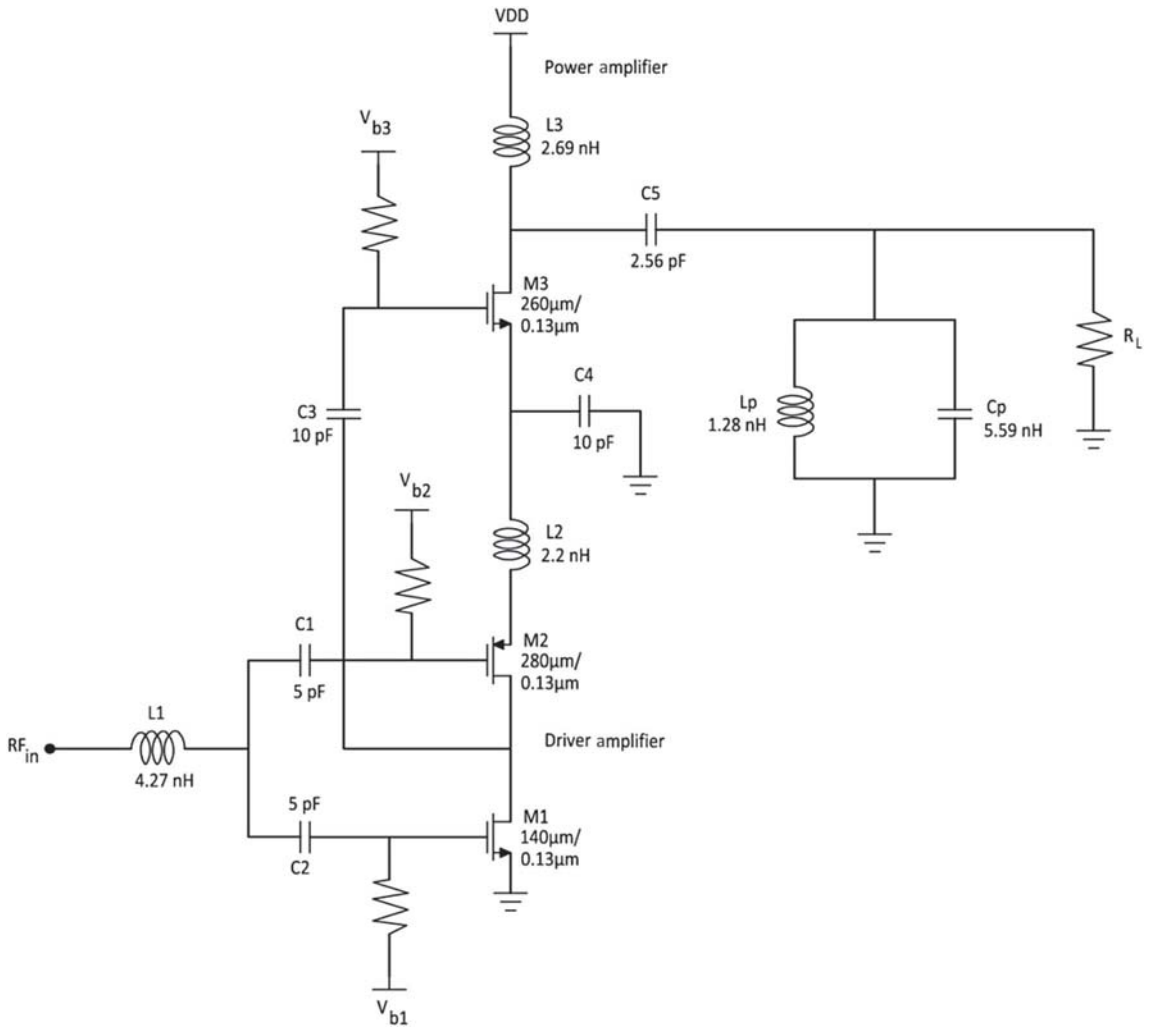

Figure 6. Schematic of power amplifier.

Eqs. (5) and (6) generate the first, second and third-order harmonics. The total drain current is calculated by adding i_0 and i_{180}, which yields

$$i_T = i_0 + i_{180} = g_2 A^2(1 + \cos 2\omega_{LO}t) + \cdots \quad (7)$$

The total current (i_T) provides DC and second-order harmonics. This differential structure doubles the LO frequency. The LC tank with NMOS switch transistor is used for low-voltage operation. The LC tank circuit is designed around 2LO frequencies to prevent the signal leakage through the power supply. The coupling capacitor is used to allow 2LO current signal from switching stage to RF stage. This LO current signal is injected into the sources of M3 and M4 transistors in RF stage. The differential RF signals (RF+ and RF−) are applied at the gates of M3 and M4 transistors. These current signals are then multiplied by the 2LO current signal to yield IF output current signal. The output differential IF voltage signals are produced by multiplication of IF current signal and its load resistance R_L.

The linearity is improved by degeneration resistor R_d, which is connected at the sources of M3 and M4 transistors of RF stage. The degeneration resistors are restricted between 30 and 150 Ω to limit the thermal noise contribution and voltage drop across them. If the degeneration resistor (R_d) is added in the RF stage, the CG becomes

$$CG = \frac{g_2 A^2}{2} \frac{R_L}{R_d + 1/g_{m1}} \quad (8)$$

If R_d value increases, CG decreases. In the proposed mixer, LO stage draws 0.4 mA DC current and the RF stage draws 0.2 mA current at a supply voltage of 0.8 V.

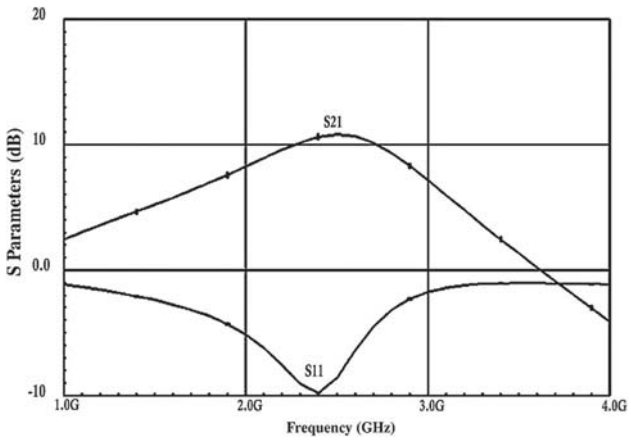

Figure 7. *S*-parameters of LNA.

3. Proposed transmitter front end

To deliver the required output power to the 50 Ω antenna, a passive subharmonic mixer, differential to single-ended converter and power amplifier (PA) are designed for supporting low power consumption.

3.1 *Subharmonic upconversion mixer*

An upconversion mixer is used for converting an IF signal to RF signal. In this paper, for supporting low power consumption, a passive mixer is proposed that does not dissipate DC current and is based on voltage switching mixers. For eliminating oscillator pulling and injection locking problems, a passive subharmonic upconversion mixer is proposed in which RF output frequency is far from the LO frequency.

A schematic of subharmonic upconversion mixer is shown in figure 4a. It contains 8 commutating switches, which are formed as stacking of two switching quads where active devices work in deep triode region. The switches are characterized by their 'on' resistance (r_{on}). These switches are controlled by quadrature LO signals. The baseband or IF differential signals are applied at the sources of LO switches. In this design, the size of switches has been chosen as 50/0.13 μm. The commutating switches upconvert the baseband or IF signal to the RF frequency signal. The LO quadrature phases of sinusoidal signal are shown in figure 4b.

In this, T is the full period of cycle. In the first quarter cycle T1, the transistors M1, M1′ and M4, M4′ are on, therefore the IF current flows to the RF port. In the second quarter cycle T2, when M1, M1' and M2, M2′ transistors are on, IF current flows to RF port but reversing the polarity. Each transistor is active for 50% of the full period of cycle T. For a single cycle, the IF current is modulated four times, and hence the LO frequency doubles, which gives the subharmonic mixing.

3.2 *Differential to single-ended converter*

The subharmonic passive upconversion mixer produces in-phase and quadrature components of RF signal, which are added to obtain the differential RF signals. To produce single-ended RF signal, an active balun circuit is designed as in figure 5.

It is composed of a two CS (differential pair) stages M1 and M2 with load resistor R1 and R2 for RF+ and RF− signals, respectively. Resistor R_s is used for tail current. The differential pairs are designed such that they perform as a balun with unity gain. Therefore, the single-ended output signal has the same amplitude as the balanced signal at the output of the mixer. The differential to single-ended converter is biased in moderate inversion

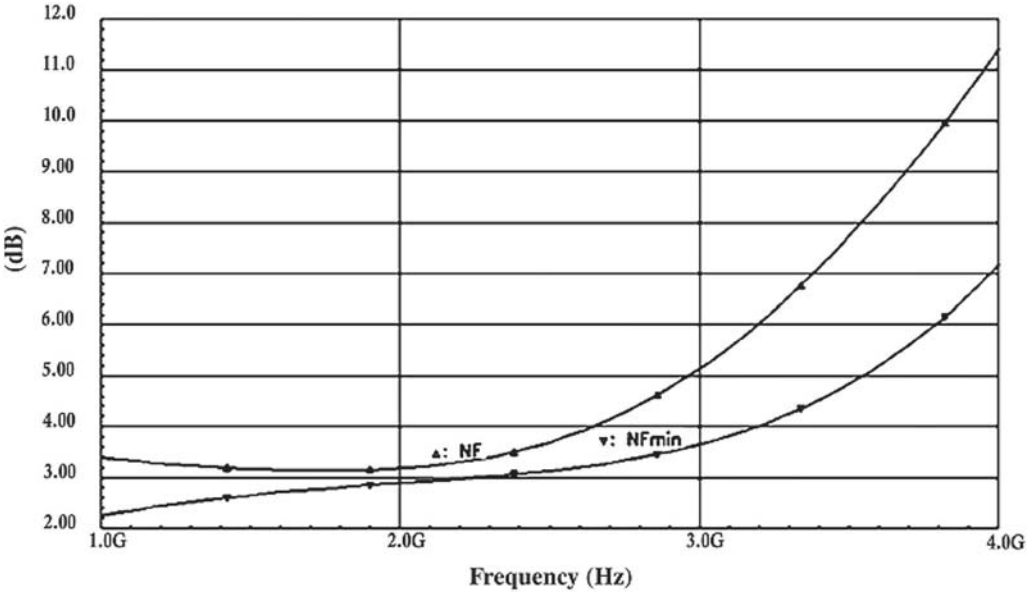

Figure 8. Noise figure of LNA.

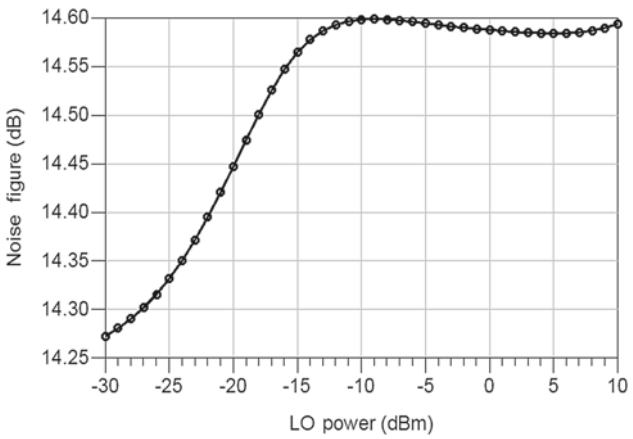

Figure 9. Noise figure of mixer.

region. It consumes 1.16 mA current from the supply voltage of 0.8 V.

3.3 *PA*

PA requires two stages for amplification. To avoid the current consumption of two stages, a single-stage current reuse class AB PA is proposed. The current reuse structure has only one current path, which supports low power consumption. In this, the power stage is stacked at the top of driver amplifier. To support low power consumption, push pull amplifier and CS amplifiers are used as the driver and PAs. A circuit schematic of PA is shown in figure 6.

The proposed single-stage class AB PA is designed using current reuse structure of driver amplifier and PA at a supply voltage of 1.2 V. In the driver amplifier, a push pull inverter is adopted to support low current. The inductor L1 and capacitors C1 and C2 are used to provide the RF input to the PA at 2.4-GHz frequency. The inductor L2 is used to provide high-impedance AC path. The output of driver amplifier is given to the input of power stage through coupling capacitor C3. In power stage, a CS class AB amplifier is used. The output matching network (C5 and parallel network L_p and C_p) is used to match 50 Ω load. This structure reduces the current consumption.

4. Results and discussion

4.1 *Receiver front end*

The integrated receiver front end which consists of LNA, balun and differential LO subharmonic mixer has been designed in 0.13 μm CMOS TSMC process. The supply voltage of entire receiver front end is 0.8 V. Subharmonic mixers are used the second-order harmonics of the LO signal. Subharmonic mixers use very attractive in direct-conversion receivers since they reduce LO self-mixing by using an LO frequency that is much lower than the RF frequency.

The LNA in receiver front end is simulated and its parameters such as *S*-parameters and noise figure are shown, respectively, in figures 7 and 8.

Single Side Band (SSB) noise figure versus LO power of downconversion mixer is plotted as shown in figure 9.

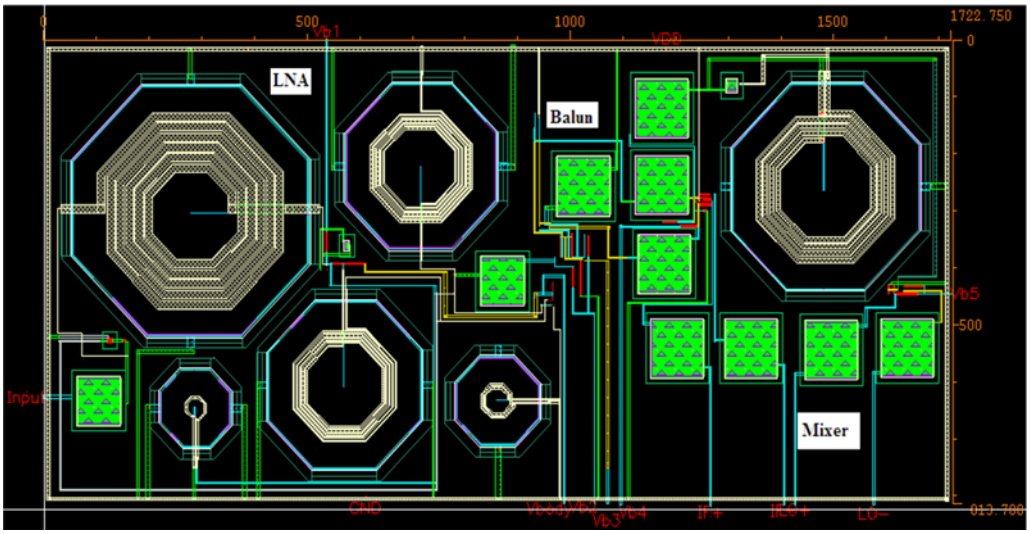

Figure 10. Layout of RF receiver front end.

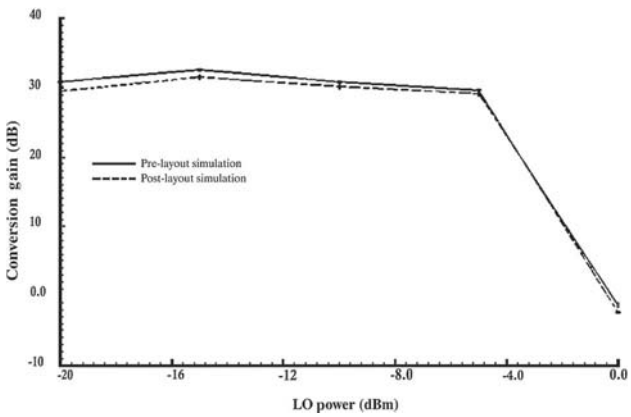

Figure 11. Conversion gain.

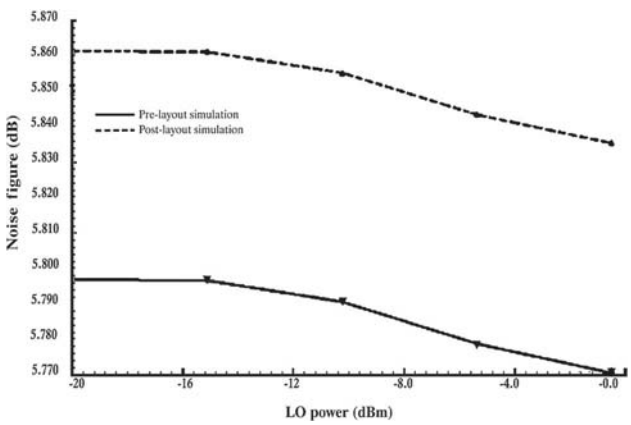

Figure 12. Noise figure of receiver front end.

Figure 10 shows the layout of receiver front end. The layout area of receiver front end is 1.4 mm^2.

The layout is simulated for high-output impedance load at IF port and the results are compared to the circuit simulation results.

The obtained CGs are 29.7 dB for circuit schematic (pre-layout) and 29 dB for layout (post-layout) at LO power of − 5 dBm as shown in figure 11. The noise figures of pre- and post-layout results are, respectively, 5.78 and 5.84 dB as shown in figure 12.

The linearity measure of IIP3 is calculated for the receiver front end. The IIP3 values of pre- and post-layout are, respectively, − 14 and − 12 dBm. The receiver front end consumes 1.79 mW power at 0.8 V supply voltage. The performance of the receiver is summarized and compared with the other works in table 1. For finding the receiver performance, Figure of Merit (FOM) is calculated to compare the performance measures of receiver front end as given in Eq. (9) [13]:

$$\mathrm{FOM}_1 = 10\log\left[\frac{10^{\mathrm{CG}/20}10^{(\mathrm{IIP3}-10)/20}}{10^{\mathrm{NF}/10}P_{\mathrm{DC}}}\right]. \qquad (9)$$

Another FOM is used to find the performance measures, which includes process technology, frequency, noise figure, power consumption and gain.

$$\mathrm{FOM}_2 = \frac{\mathrm{CG(dB)freq(GHz)gatelength(nm)}}{\mathrm{current(mA)NF\ (dB)}}. \qquad (10)$$

4.2 *Transmitter front end*

For the transmitter, the IF signal of 5 MHz and 1.2-GHz LO signals are applied to the upconversion mixer, which

Table 1. Performance comparison of receiver and transmitter front end.

	Receiver front end					Transmitter front end	
Specifications	[8]	[9]	[10]	This work	Specifications	[12]	This work
Frequency (GHz)	2.4	2.4	2.45	2.4	Frequency (MHz)	900	2400
Technology (nm)	180	130	90	130	Technology (nm)	180	130
Supply voltage (V)	1.8	1.2	1.2	0.8	Supply voltage (V)	1.2	0.8–1.2
Noise figure (dB)	8.9	2.27	9.3	5.84	Output power (dBm)	0	0
Conversion gain (dB)	8	16.7	30	29	Conversion gain (dB)	16 @ PLO = 0 dBm	15 @PLO = − 5 dBm
IIP3 (dBm)	− 13.5	∼ − 9.8	− 9.8	− 12	OP-1 dB (dBm)	3	0
Power consumption (mW)	2.75	5.5	4.16	1.79	Power consumption (mW)	5	4.27
FOM_1 (dB)	8.95	18.77	19.6	25.13	FOM_1 (dB/mW)	3.2	3.51
FOM_2	141	417	171	866	FOM_2	518	3468

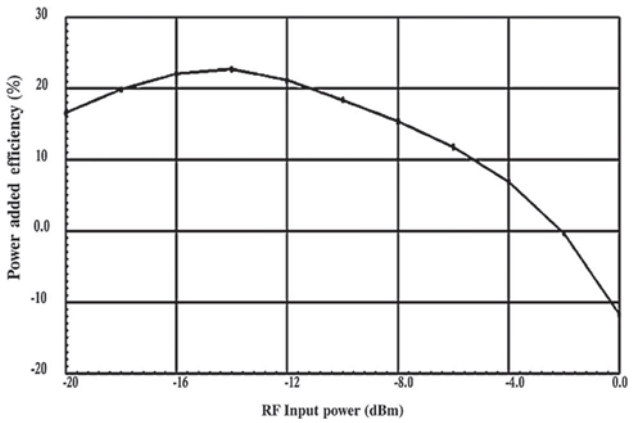

Figure 13. Power added efficiency of PA.

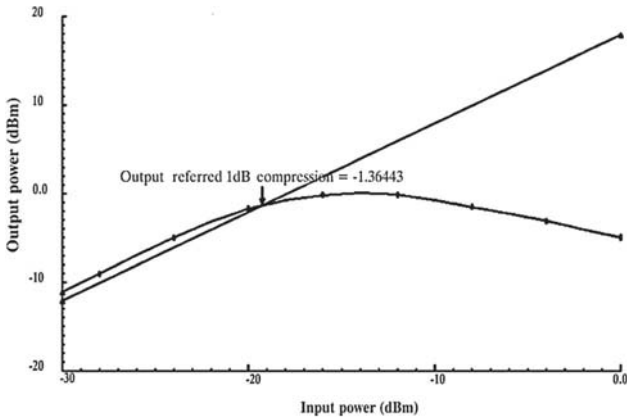

Figure 15. Output 1-dB compression point.

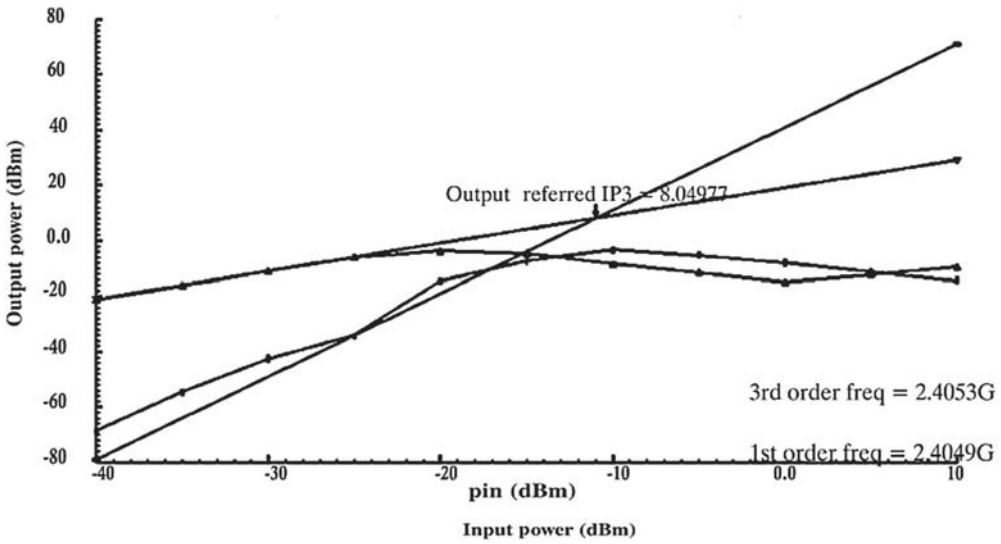

Figure 14. Output intercept point.

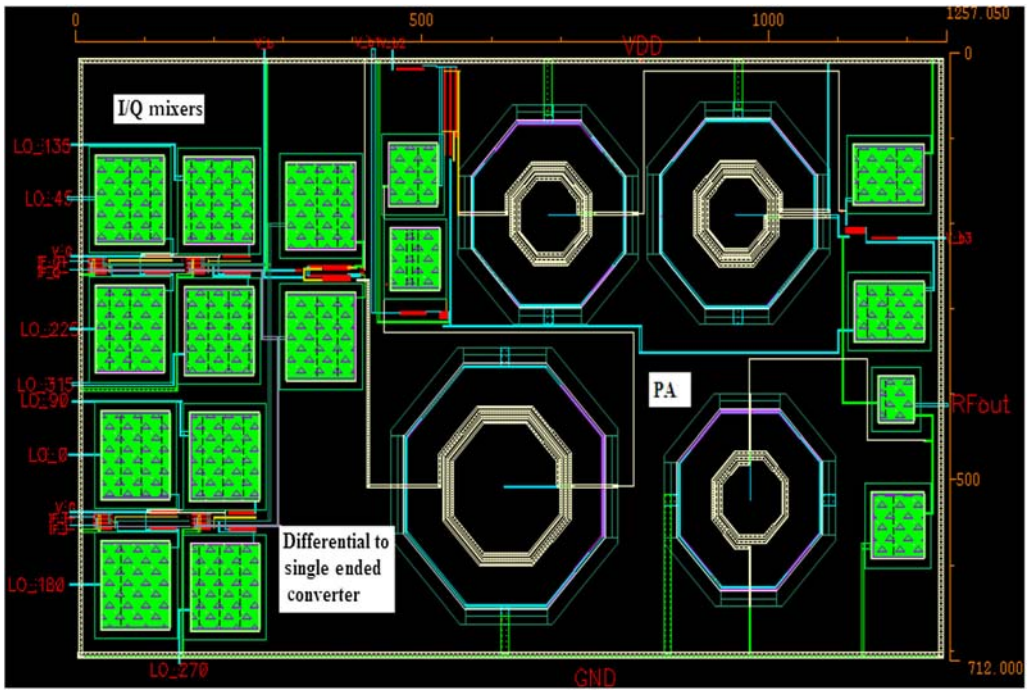

Figure 16. Layout of transmitter front end.

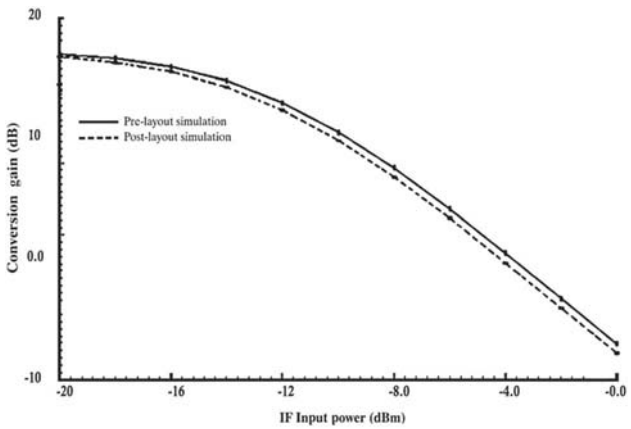

Figure 17. Conversion gain of transmitter front end.

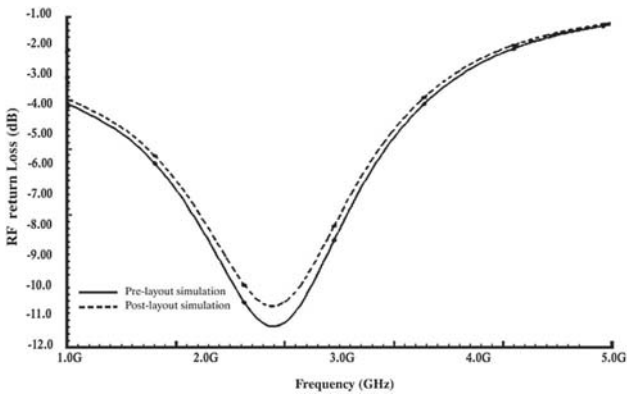

Figure 18. Output return loss of transmitter front end.

produces the RF signal. This RF signal is amplified to achieve the 0-dBm output power. PA is simulated and it produces 19.8% of power added efficiency at the designed output power of 0 dBm as shown in figure 13.

OIP3 of 8 dB is obtained as seen in figure 14. OP1dB of − 1.36 dBm is observed as shown in figure 15.

The layout of the direct conversion transmitter has been drawn as shown in figure 16. It occupies an active area of 0.894 mm^2.

Figure 17 shows the overall CG of the transmitter front end versus IF power. The pre- and post-layout simulation produces the conversion gain of, respectively, 15.5 and 15 dB when the LO power is − 5 dBm and consumes 4.27 mW power consumption under the 1.2 V supply voltage.

For the transmitter, output return loss ($S(2,2)$) of, respectively, − 11 and − 10.3 dB are obtained for pre- and post-layout simulation as shown in figure 18. The output return loss indicates the good RF output matching condition.

Also, the transmitter front end achieves, respectively, − 0.915 and 0 dBm of OP-1 dB for pre- and post-layout simulations as shown in figure 19.

The performance of the transmitter is summarized and compared with [12] in table 1. For finding the transmitter

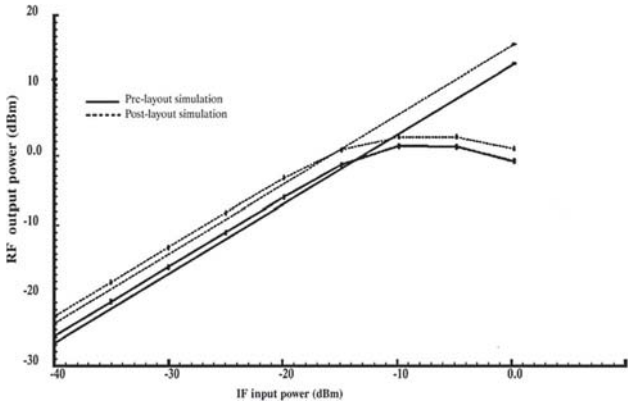

Figure 19. Output 1-dB compression point.

performance, FOM_1 and FOM_2 are calculated to compare the performance measures of transmitter front end as given in Eqs. (11) and (12):

$$FOM_1 = {}^{CG\ [dB]}/_{power\ consumption\ [mW]} \tag{11}$$

$$FOM_2 = \frac{CG\ (dB)freq\ (GHz)gatelength\ (nm)}{power\ (mW)P_{LO}(mW)}. \tag{12}$$

Table 1 summarizes the performances of receiver and transmitter front ends with the existing works.

When compared with the simulation results of other receivers, the noise figure and power consumption of proposed receiver are improved. The area of the layout is increased to 1.4 mm^2 because 57% of area is occupied by LNA, which uses a large number of inductors to achieve good performance at low power. The proposed receiver front end has achieved good FOM of 25.13. The receiver front end has produced better performances in terms of CG, noise figure, IIP3 and power consumption.

In [12], the transmitter post-layout results are $\pm$ 1 dB deviation of the measurement results, which are presented in table 1. The power consumption has reduced at low LO power in the proposed transmitter. FOM is calculated as the ratio of gain to the power consumption. The performance of proposed work is compared to the existing work using FOM. Though the FOM of proposed transmitter is very slightly increased than that of the existing work, the proposed transmitter has mitigated the LO pulling problem. The transmitter has achieved 0 dBm output power at 4.27 mW DC power consumption.

5. Conclusion

Direct conversion transmitter and receiver front ends are designed and simulated at 2.4-GHz frequency using the TSMC 0.13 μm CMOS process. Subharmonic mixers are designed at the transmitter and receiver to avoid the drawbacks of direct conversion transceiver such as self-mixing, DC offsets and LO pulling problem. In this work, subharmonic mixers are used as second-order harmonics of the LO signal. The receiver front end has achieved a voltage gain of 29 dB, a noise figure of 5.84 dB and input IP3 of $-$ 12 dBm. The transmitter front end has produced 15 dB CG and 0 dBm OP1dB, and consumes 4.27 mW power for achieving 0 dBm of output power. The proposed low-power transceiver front end is more suitable for short-range wireless communications.

Abbreviations

CG	Conversion gain
P_{LO}	Local oscillator power
OP-1	Output 1-dB compression point
IIP3	Input 3rd-order intercept point
ω_{LO}	Local oscillator frequency
P_{DC}	DC power consumption
$S(2,2)$	Output return loss
$S(1,1)$	Input return loss
NF	Noise figure

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