Synchronous programmable divider design for PLL Using 0.18 um cmos technology

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Abstract

In the wireless communication market, trends are moving towards smaller size, fewer parts, longer lifetime and higher frequency operation. These trends imply that wireless communications circuits must incorporate higher integration and that their design and IC technology must be optimized for low power and high frequency system. One innovative method to increase the frequency of programmable divider is discussed. The new method not only increases the frequency of operation but also decreases circuit complexity and power dissipation. This new design use synchronous counters instead of asynchronous counters. The digital gates are optimized for minimum propagation delay and loading effect using progressive sizing of the transistors. This is better configuration in every aspect in terms of frequency, power dissipation and chip area.

Index terms: *CMOS integrated circuits, frequency synthesizers, phase locked loop, programmable divider, Prescaler, PLL.*

1. Introduction

The scaling of CMOS technologies to deep submicron has made CMOS a technological option for the low-gigahertz frequency range. However, for CMOS to become a commercial option for RF building blocks requires compliance to all trends of the consumer market: miniaturization, low cost, high reliability and long battery lifetime. Bulk CMOS technologies presently available satisfy the low cost and reliability trends by standard design practice. Complying with miniaturization and long battery lifetime, on the other hand, demands CMOS building blocks with low-power dissipation and good electromagnetic compatibility (EMC) characteristics. A critical RF function in this context is the frequency synthesizer, more particularly the programmable frequency divider. The divider consists of logic gates Which operate at RF frequency, Due to the divider's complexity, high operation frequency normally leads to high power dissipation. Other crucial aspects of the present-day consumer electronics industry are the short time available for the introduction of new products in the market, and the short product lifetime. On top of that, the lifespan of a given CMOS technology is also short, due to the aggressive scaling of minimum feature sizes. Short time-to-market demands architectures providing easy optimization of power dissipation, fast design time and simple layout work. High reusability, in turn, requires an architecture, which provides easy adaptation of the input frequency range and of the maximum and minimum division ratios of existing designs.

The choice of the divider architecture is therefore essential for achieving low-power dissipation, high design flexibility and high reusability of existing building blocks. A modular architecture complies with these requirements, as shall be demonstrated in this paper.

The divider can be implemented using static or dynamic cmos circuits. Dynamic circuit techniques evolved in the last few years into several cmos circuit technique such as domino, NORA, TSPC circuits. Nevertheless, the field of CMOS integrated circuits has reached a level of maturity, where it is now mainstream technology for higher integration density, low power consumption. Therefore, we had chosen cmos to design the programmable divider. The designed dividers have increased frequency capability with reduction of propagation delay using synchronous counters instead of asynchronous counters. The focus of the paper is first on the truly modular architecture and on the implementation of the circuits. Then the description of circuits with their behavior inside the programmable divider is described. Finally, a collection of measured data and the conclusions are presented.

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2. Background

Phase-Locked Loops (PLL) is standard components on almost all-modern Integrated Circuits. Their uses range from frequency synthesis (i.e. to increase or decrease the period of a given periodic signal), to data recovery, to minimizing clock skew on large ICs.

Because of the extreme importance of PLL in today's architectures, a great deal of research and literature on the topic emanates from some of the top minds in the IC industry and the academic field. The current state of knowledge of general PLL mathematical interpretation, design and fabrication is vast; however, research does not exist for the design of a PLL in the specific implementation we are proposing. PLL is very challenging because internal circuits must be both digital and analog. In fact, although both the inputs and outputs of the PLL are digital signals, all internal circuitry is essentially analog. It is the analog areas of the PLL that require the most design experience and are the most difficult to test.

3. PLL Overview

The function of the PLL is to lock the phase and frequency of the VCO to the reference oscillator. The VCO output is coupled into the PLL circuit where the VCO frequency is divided down in a dual modulus Prescaler and feed back divider to the phase comparison frequency or step size of PLL. The block diagram of PLL is shown in figure 1. The shaded portion is the programmable divider section.

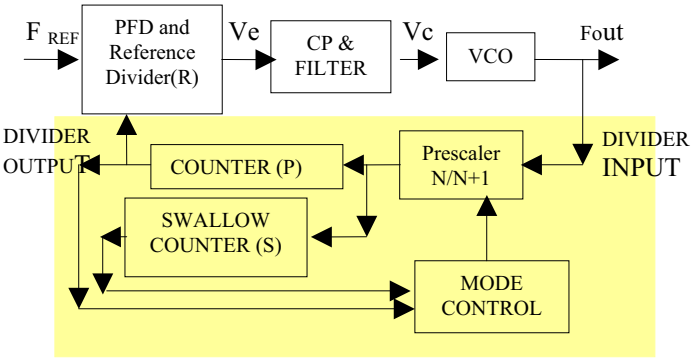

Figure 1: Block diagram of PLL

4. Design Requirement

The synthesizer generates frequencies in the range of 2.4 to 2.5GHz in steps of 1MHz. The synthesizer architecture is given in figure 1. This is a single-loop PLL. VCO oscillates in the range of 2.4 to 2.5GHz and gives out a frequency component proportional to the control voltage input. The programmable divider N divides the VCO frequency. The PFD compares the Phase & frequency of the VCO-divided-by-N and the reference-divided-by-'R' signals and applies a correction voltage to the VCO tuning input. This keeps the VCO phase locked to the reference.

Dual modulus prescaler and the counters 'P' & 'S' form the programmable divider. This divides the VCO output to 1 MHz. Their operation is as follows. The prescaler divides the VCO frequency output by 17 until 'S' counter counts down to zero. At this point, it switches over and divides by 16 until 'P' counter counts down to zero. Then the counters are reloaded and the DMP switches back to divide-by-17. External crystal oscillator provides a stable reference of 10MHz that is internally divided down by the 'R' counter to 1MHz.

PFD and charge pump in combination with the external loop filter give out a voltage proportional to the phase or frequency difference between the reference and the divided VCO output. The external loop filter establishes the Phase noise of the synthesizer output, the locking time and suppression of reference spurii.

Frequency setting: 'P', 'S' & 'R' are programmable counters. Loading 'P', 'S' & 'R' counters (fig.1) set the synthesizer frequency. Three 9-bit latches are present, which load the counters every time they count down to '0'. A 9-bit control word is programmed into the latches from external glue logic. Two latch-select bits and a strobe are used. Hence, 12 pins (9 data pins + 2 latch select + 1 strobe) are required for programming.

5. 9 bit Programmable divider

There are three programmable dividers in this PLL chip. We will discuss one programmable divider. The other two dividers are implemented in the same manner. Such a programmable divider consists of three parts. The block diagram of 9 bit programmable divider is shown in figure 2. It has N bit counter, control logic and SR latch. After the

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loaded (programmed value) the out put of the control logic will be one and all the flip flops are cleared.

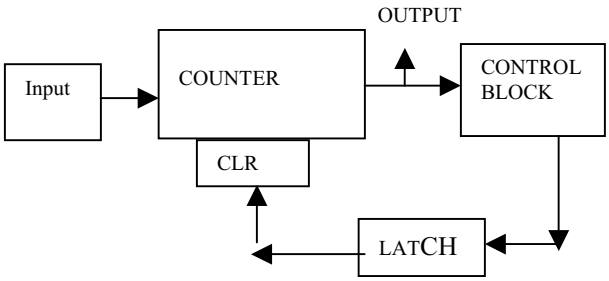

Figure 2: 9 bit programmable divider

The function of the 9 bit divider is based on digital logic. The counter can be synchronous or asynchronous down counters. The control logic is used to load the desired value. The counters are down counters. The divider output is taken across MSB of the counters. For normal operation the input clock frequency is divided by 512 (9 bit). But in order to divide the frequency for the programmed value, the counter is to be cleared after the loaded value. The function of the control block is to generate signal for counters to be cleared. .

The schematic of the control block is given in figure 3. It consists of two input XOR gates. As we know if the two inputs of the XOR gate are same then output is zero otherwise it is one. We use this principle for our divider design. For 9 bit divider we need nine two input XOR gates. One input of the XOR gate is used for loading and the other input is for comparing with QB output of individual flip flops of the counter. When all the loaded value is equal to all QB then all the output of the XOR gates are zero and the output of nor gate is one. The output of the NOR gate is used to clear the flip flops.

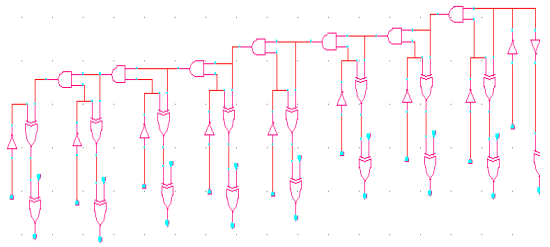

Figure 3: Control circuit for 9 bit programmable divider

With this control circuit of XOR gates having comparison of QBAR of individual flip flops will give divided output frequency by loaded value minus one. Therefore, we had added an incrementer circuit in the divider circuit, so that the output frequency will be divided by the loaded value.
Here, first we invert the loaded value, then we increment by one using incrementer. Without the incrementer the output frequency is divided by loaded value minus one.

To get a clear picture of the function of the divider take for example design of 4 bit programmable divider. It consists of one 4 bit synchronous counter and control block. The outputs of the counters are QB4, QB3, QB2, and QB1. The MSB is QB4, For normal operation the QB4 is divided form of the clock by 15. If we are loading 3 (0011) then it will be inverted to 1100 and incremented by one so the final value is 1101. So when the counter value reaches at 1101, then all the flip-flops will be cleared. So we will get three clocks, 1111 to 1101 high value and one low value. So in total there are three clock means the frequency of the clock is divided by three, which is the loaded value.

But the propagation delay from the output of control circuit to the control input of individual flip-flop will vary, so the clear of all the flip-flops will not occur simultaneously. The last flip flop (MSB of counter) will take appreciably longer time to reset than the first flip flop. Wide variations in reset propagation time will occur if the counters are unevenly loaded. A method of eliminating this difficulty with resetting is to use a latch to memorise the output of nand gate at the Nth pulse. This process is termed as pipelining of the flip flops. The complete schematic of the 9 bit divider is shown in figure 4.

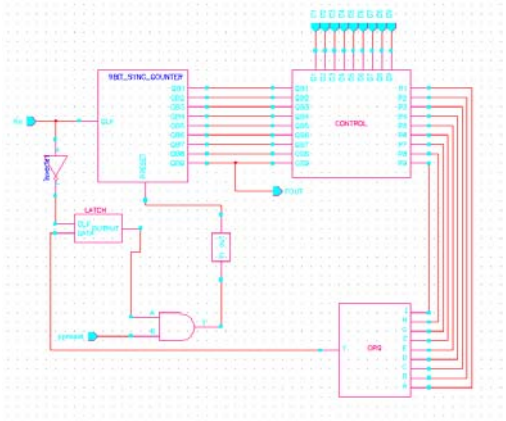

Figure.4: Schematic of 9bit programmable divider

6. Programming overview

The programmable dividers are serially programmed using a standard serial input parallel

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output (SIPO) shift register. The programming data is input using the clock; data and latch enable input pins. The clock input latches one bit on the data input into PLL shift register on the rising edge of each clock pulse. When the latch enable input is high, the stored data is transferred into the latches. Then the programmable divider is loaded with the programmed value and is in the same value until unless the latch enable is high.

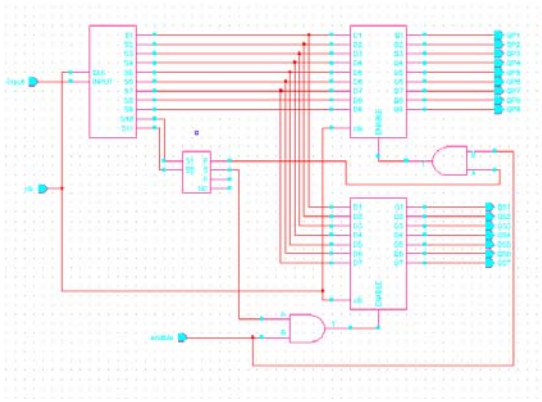

Figure 5 Schematic of programming section of programmable divider

The schematic is shown in figure 5. Here we used 11 bit shift register to load the dividers. The first nine bit will decide the loaded value for the divider and the last two bits will select the dividers (P/S or R) The last two bits are given to a decoder inputs, which will send enable to the individual dividers. If it is (0,1) the divider P is selected, If it is (1,0) then divider S will be selected and if it is (0,0) then divider R will be selected.

7. Circuit Design

The programmable dividers are designed using TSMC 0.18um technology. As all the circuits are digital only, so we chose CMOS process instead of BICMOS or SiGe. So also the preliminary analysis of the 0.18um technology was verified to meet the design requirements. The design requirements for the programmable divider is given in table-1

Table 1 Design requirement for programmable divider

Parameter	Specification	Unit
	Min	Typ	Max	
Power supply	1.65	1.8	1.9	Volt
Input frequency ('S','P')			400	MHz
Output freq. ('S','P')			25	MHz
'HIGH' voltage	$0.7V_{dd}$			V
'LOW' voltage			$0.2V_{dd}$	V
'S' counter	0		127	
'P'	3		511	
'R'	3		127	

First, the functionality of the programmable divider is tested using AHDL models. The uses of AHDL models have mainly two advantages. One is the simulation time is less for AHDL models against using transistor models directly. The second is it is easy to change the specifications of the models to meet the design requirement.

Then all the AHDL models are replaced with transistor models one by one. In each and every change, the functionality is tested thoroughly. The circuit diagram of the programmable divider is shown in figure 6. Each block is already explained previously. So also, these are fundamental building blocks for a digital designer. The circuits are self explanatory.

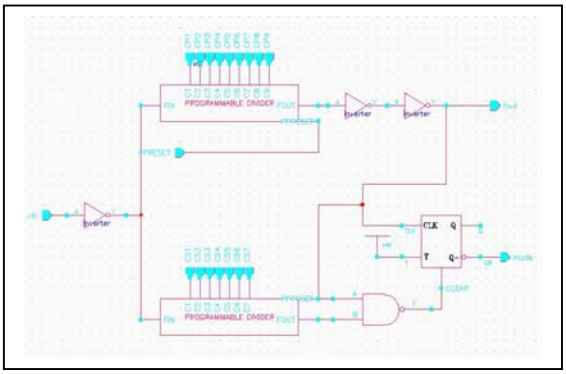

Figure.6: Schematic of the divider without the programming section.

8. Characterization

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The programmable divider is completely characterised with different process, temperature and power supply variations from normal conditions. The programmable divider is tested with interfacing with a general bit pattern generator. The general bit pattern is implemented using AHDL models. The property of the generator allows the user to generate any loading value depending upon the user. The schematic of the complete programmable divider with testing part is shown in figure 7.

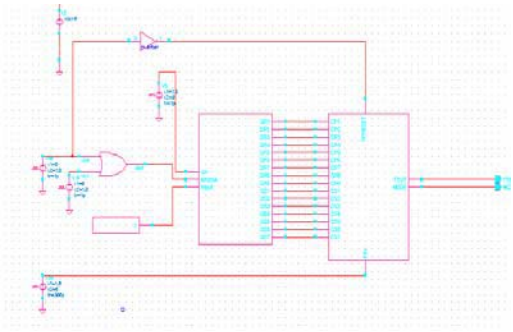

Figure 7: Schematic of programmable divider for characterization.

The simulation is carried out under worst case conditions. The divider is tested using slow slow (SS) corner analysis, 50 degree centigrade temperature and power supply of 0.2V low to 1.6 V high. The simulation is carried out both in schematic and parasitic extraction level of the programmable divider with application of all the worst-case conditions at the same time. The simulated graph is shown in figure 8, It shows the divided output for P=7 and S=3. This output will go to mode control circuit of prescaler. For low level the prescaler will select N+1 and for high logic it will select N. The design of prescaler is not part of this research. So the design of prescaler is excluded here. We had concentrated of the divider section of the PLL without the prescaler.

The programmable divider is characterised with different values of P and S, The layout is shown in figure 9. The simulation on parasitic extraction is working well above 2.85nS, whereas the schematic level simulation is working at 2.5nS. The variation in the frequency is due to RC delay of the divider in the interconnections and parasitic.

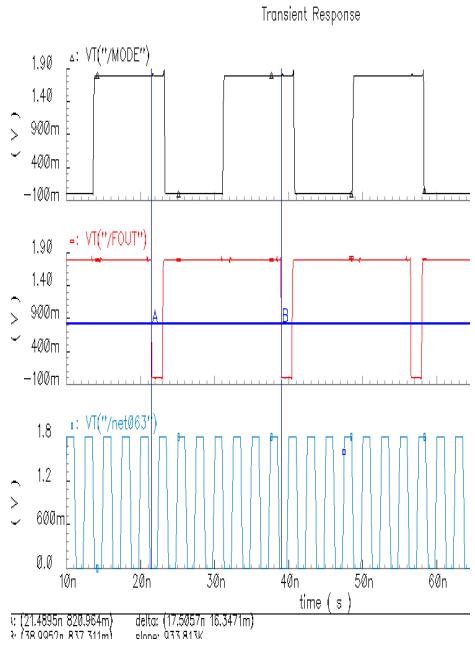

Figure 8: Simulated output of the divider for input clock period 2.5nS and P=7 and S=3

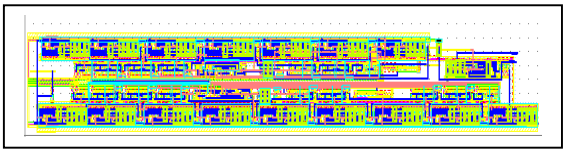

Figure.7: layout of the Programmable divider

Figure 9: Layout of the divider

9. Conclusion

The architecture, principle and circuit design of the programmable divider was described here. From the simulation results it is clear that the designed programmable divider meets all the specifications except the frequency requirement. The difference in delay between schematic and parasitic simulation can be minimize. As we had concentrated on less chip area and less power dissipation, so the propagation delay is little bit more. However for decreasing the delay, we have to pay for the higher power dissipation. The future development will be in terms of further increase of application frequency, power dissipation and area.

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Reference

[1]. J. Craninckx and M. S. J. Steyaert, "A 1.75-GHz/3-V Dual- Modulus Divide-by-128/129 Prescaler in 0.7-_m CMOS",*IEEE Journal of Solid State Circuits*, vol. 31, no. 7, pp. 890- 897, July 1996.

[2] J. Yuan and C. Svensson, "High-Speed CMOS Circuit Technique ",*IEEE Journal of Solid-State Circuits*, vol. 24, no. 1,pp. 62-70, Feb. 1989.

[3] J. Craninckx and M. Steyaert, "A 1.75 GHz/3 V dual-modulus divide-by-128/129 prescalar in 0.7 _m CMOS," IEEE J. Solid-State Circuits, vol. 31, pp. 890–897, July 1996.

[4] F. Piazza and Q. Huang, "A low power CMOS dual modulus prescaler for frequency synthesizers," IEICE Trans. Electron., vol. E80-C, pp. 314–319, Feb. 1997.

[5] P. Larsson, "High-speed architecture for a programmable frequency divider and a dual-modulus prescaler," IEEE J. Solid-State Circuits, vol. 31, pp. 744–748, May 1996.

[6] J. Navarro Soares, Jr. and W. A. M. Van Noije, "A 1.6 GHz dual-modulus prescaler using the extended true-single-phase-clock CMOS circuit technique (E-TSPC)," IEEE J. Solid-State Circuits, vol. 34, pp. 97–102, Jan. 1999.

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